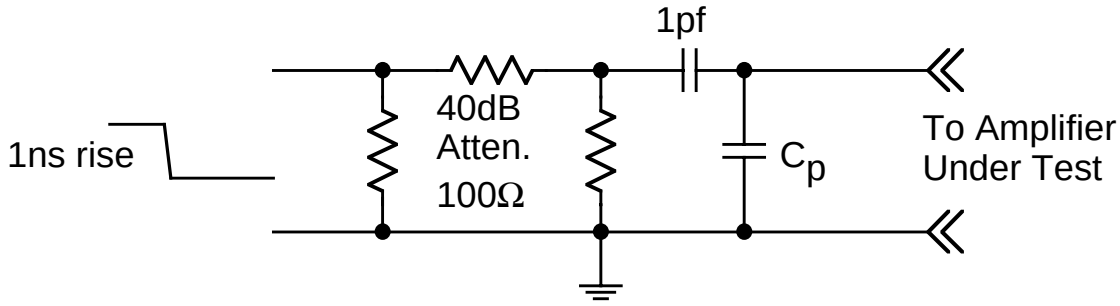
UMS Chamber Electronics Progress

Test UPENN ASDQ (used by CDF) and an Amplifier + Shaper/Discriminator built from commercial parts.

Measure

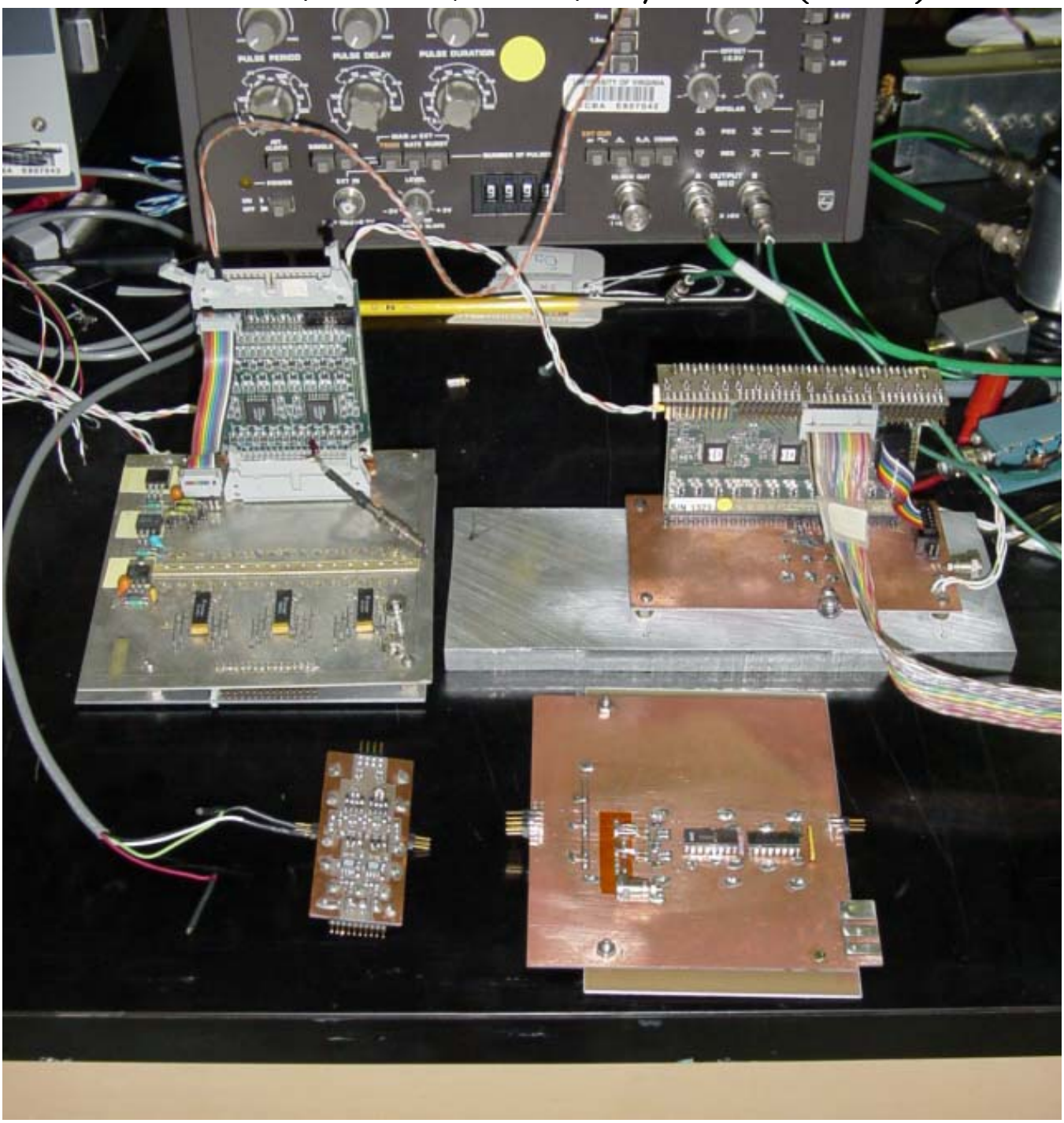
- ENC: Equivalent noise charge at input
- T_r: time slewing 20% – 90%

Test input is $\delta-$like current impulse:



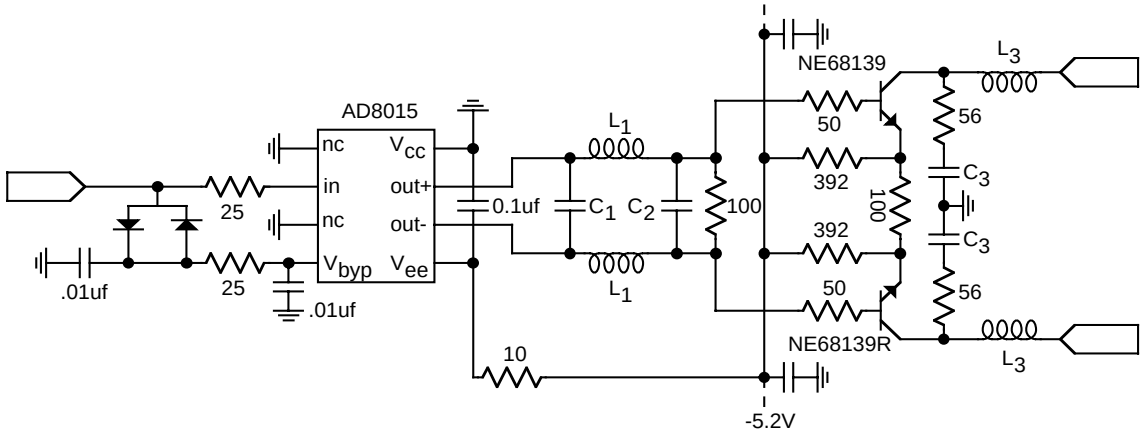
$C_p = 0 - 22$ pf simulates chamber capacitance.
(Measured FANOUT board capacitance $= 10-12$ pf)

Test setup for HyperCP amp, UPENN-ASDQ and Amplifier + Shaper/Discr (ASD)

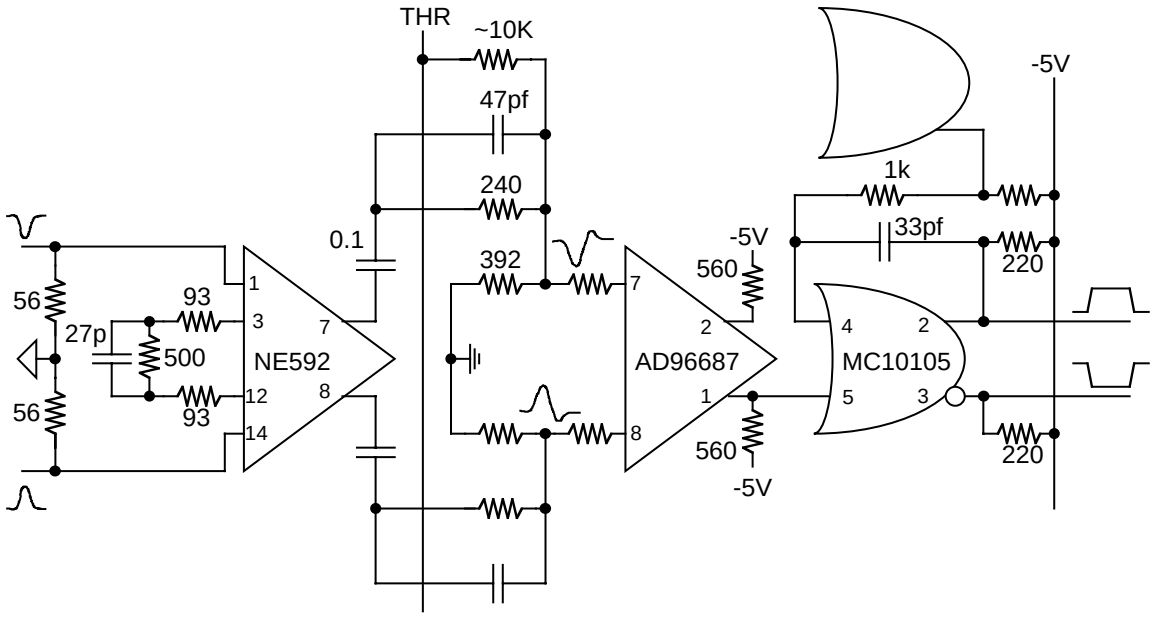


ASD using Commercial Parts

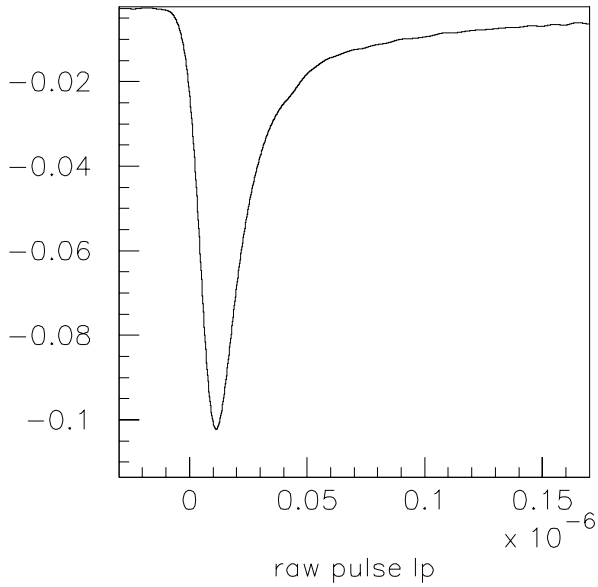
- PREAMP: TIA followed by 4^{th} order low-pass $\tau_{LP} = 2-3\,\text{ns}$



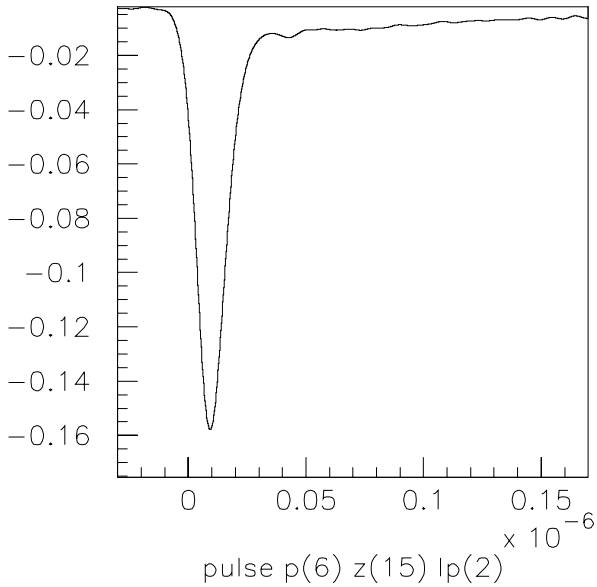
- SHAPER: cancel ion-tail $\tau_\circ = 1\,\text{ns}$ (see SLP meeting)
- DISCR: "Burst Guard" timing output; width= max(20ns, TOT)



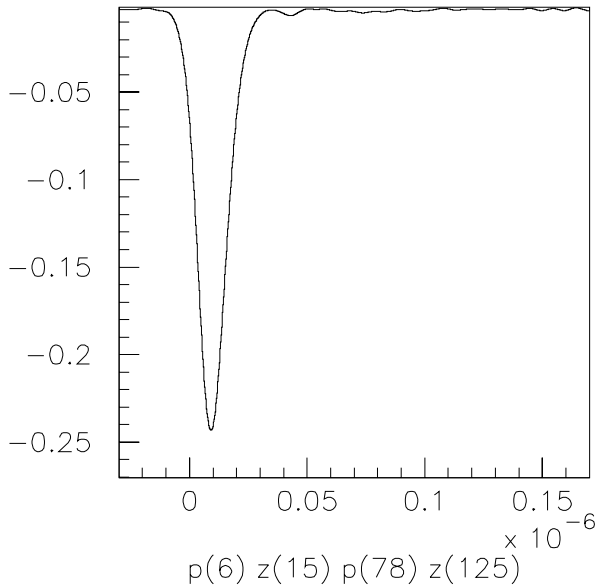
From SLP Meeting: two P/Z stages cancels ion-tail



raw pulse lp

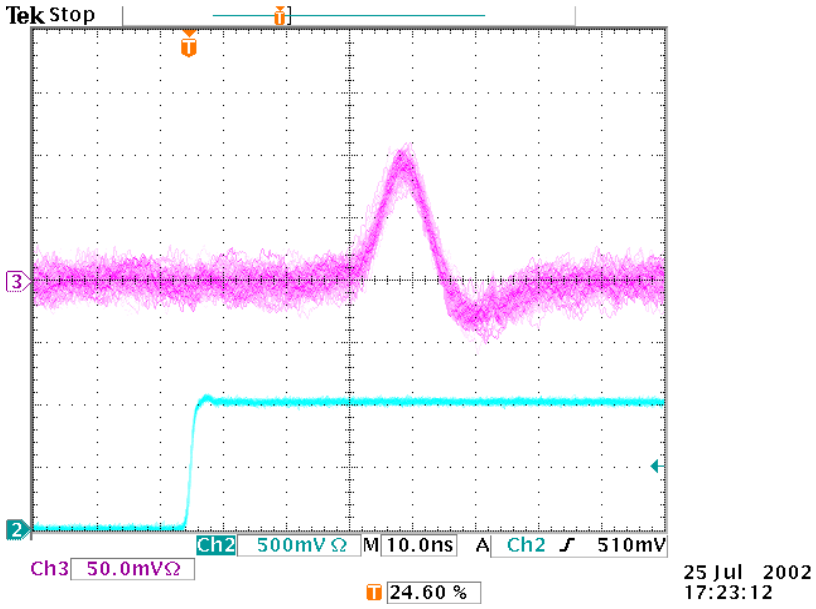


pulse p(6) z(15) lp(2)

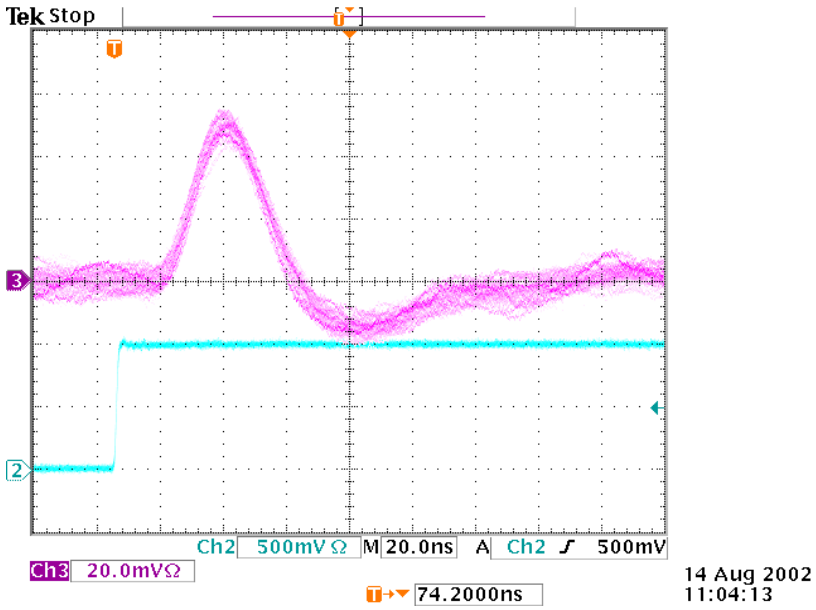


p(6) z(15) p(78) z(125)

Signal at ASD Shaper output with $C_p = 22\,\text{pf}$

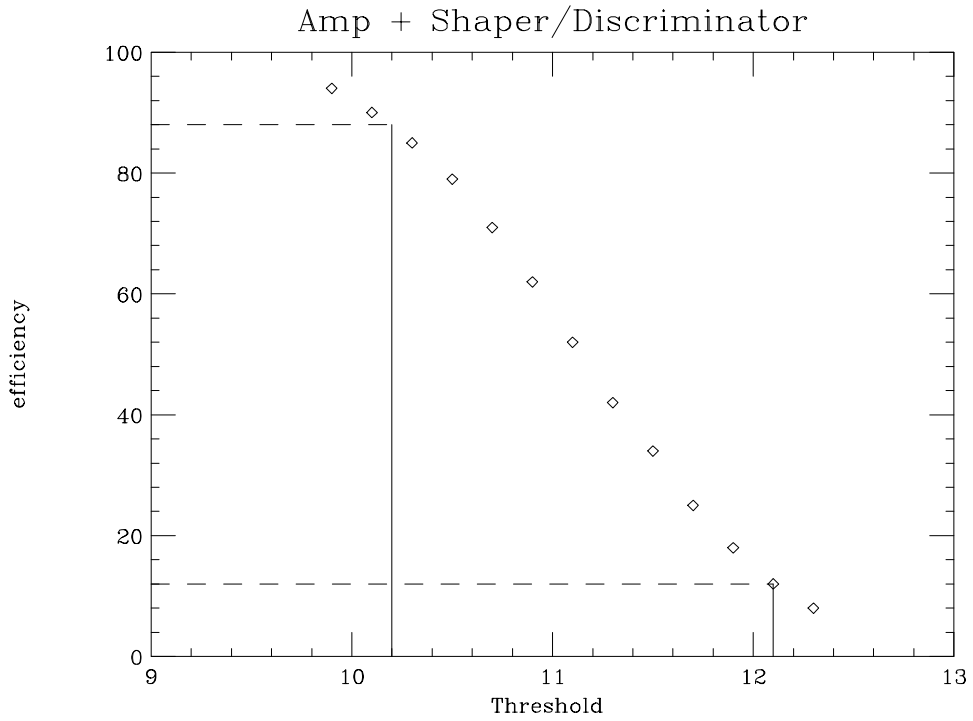


Hypercp amplifier includes shaper:
ENC $\sim$ 0.5fC, but $T_r \sim$ 12ns.



Measurement Details:

- $ENC = \frac{1}{2.35} \times \frac{V(12\%) - V(88\%)}{G_Q}$



- $T_r = T|_{Q_{thr}=.9Q_{in}} - T|_{Q_{thr}=.2Q_{in}}$ for $Q_{in} = 10$fC.

Results

	C_p=0pf		C_p=22pf	
	ENC [fC]	T_r [ns]	ENC [fC]	T_r [ns]
UPENN-ASDQ	0.29	4.8	0.61	5.4
COM-ASD (2ns)	0.20	3.6	0.81	4.8
COM-ASD (3ns)	0.20	4.0	0.68	4.8

Goals: ENC$\sim$0.5fC and $T_r \leq$ 6ns (width $\leq$ 20ns)

Future direction

Amplifier:

$\Rightarrow$ try increasing τ_{LP} in current amplifier

$\Rightarrow$ investigate other Transimpedance amplifier ICs

$\Rightarrow$ fallback – discrete transistors

Shaper/Discriminator:

$\Rightarrow$ speedup cap. discharge

$\Rightarrow$ implement LVDS output

$\Rightarrow$ reduce power (try TTL-LDVS version)